

# DATA SHEET

## **BSH301**

Dual N-channel enhancement  
mode MOS transistor

Objective specification

1999 Apr 06

Dual N-channel enhancement mode MOS transistor

BSH301

FEATURES

- 40 mΩ on-state resistance at 2.5 V gate drive
- $R_{DSon}$  rating down to 1.8 V
- ESD gate protection.

APPLICATIONS

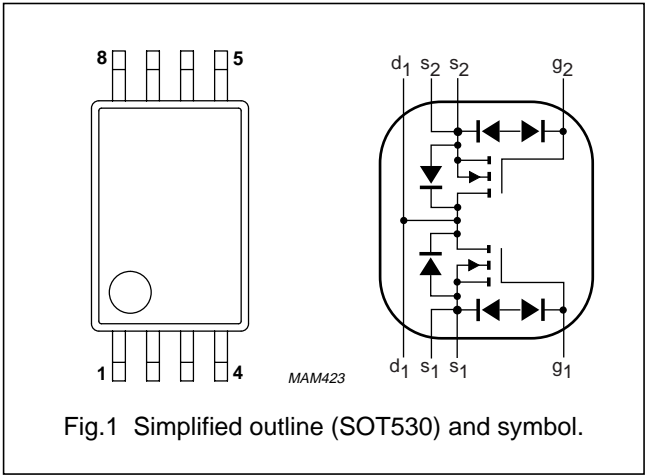
- Li-Ion safety switch
- Power management.

DESCRIPTION

Two N-channel enhancement mode MOS transistors in an 8-pin plastic TSSOP8 package.

PINNING SOT530 (TSSOP8)

PIN	SYMBOL	DESCRIPTION
1	d1	drain 1
2	s1	source 1
3	s1	source 1
4	g1	gate 1
5	g2	gate 2
6	s2	source 2
7	s2	source 2
8	d1	drain 1



CAUTION

The device is supplied in an antistatic package. The gate inputs must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		–	20	V
$V_{SD}$	source-drain diode forward voltage	$V_{GD} = 0$ ; $I_S = 1.25$ A	–	1	V
$V_{GS}$	gate-source voltage (DC)		–	±8	V
$V_{GSth}$	gate-source threshold voltage	$V_{DS} = V_{GS}$ ; $I_D = 1$ mA	0.4	–	V
$I_D$	drain current (DC)	$T_S = 80$ °C; note 1	–	5	A
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 2.5$ V; $I_D = 3.5$ A	–	0.04	Ω
$P_{tot}$	total power dissipation	$T_S = 80$ °C	–	1.75	W

Note

1.  $T_S$  is the temperature at the soldering of the drain lead.

Full Data Sheet will appear: on WWW (Internet; details in front section/back of this HB/CD-ROM) or updated Loose leaf

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per FET</b>					
$V_{DS}$	drain-source voltage (DC)		–	20	V
$V_{GS}$	gate-source voltage (DC)		–	$\pm 8$	V
$I_D$	drain current (DC)	$T_S = 80\text{ }^{\circ}\text{C}$ ; note 1	–	5	A
$I_{DM}$	peak drain current	note 2	–	20	A
$P_{tot}$	total power dissipation	$T_S = 80\text{ }^{\circ}\text{C}$ ; note 3	–	1.75	W
		$T_{amb} = 25\text{ }^{\circ}\text{C}$ ; note 4	–	1.85	W
		$T_{amb} = 25\text{ }^{\circ}\text{C}$ ; note 5	–	0.95	W
$T_{stg}$	storage temperature		–55	+150	$^{\circ}\text{C}$
$T_j$	operating junction temperature		–55	+150	$^{\circ}\text{C}$
<b>Source-drain diode</b>					
$I_S$	source current (DC)	$T_S = 80\text{ }^{\circ}\text{C}$	–	1.75	A
$I_{SM}$	peak pulsed source current	note 2	–	7	A

**Notes**

1.  $T_S$  is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per transistor. Both devices may be loaded up to 3.5 W at the same time.
4. Maximum permissible dissipation per transistor. Device mounted on a printed-circuit board with  $R_{th\ a\text{-tp}}$  (ambient to tie-point) of  $27.5\text{ }^{\circ}\text{C/W}$ .
5. Maximum permissible dissipation per transistor. Device mounted on a printed-circuit board with  $R_{th\ a\text{-tp}}$  (ambient to tie-point) of  $90\text{ }^{\circ}\text{C/W}$ .

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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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**Argentina:** see South America

**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

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**Bulgaria:** Philips Bulgaria Ltd., Energoproject, 15th floor,  
51 James Bourchier Blvd., 1407 SOFIA,  
Tel. +359 2 68 9211, Fax. +359 2 68 9102

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Tel. +1 800 234 7381, Fax. +1 800 943 0087

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
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Tel. +852 2319 7888, Fax. +852 2319 7700

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**Czech Republic:** see Austria

**Denmark:** Sydhavnsgade 23, 1780 COPENHAGEN V,  
Tel. +45 33 29 3333, Fax. +45 33 29 3905

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615 800, Fax. +358 9 6158 0920

**France:** 51 Rue Carnot, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Band Box Building, 2nd floor,  
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,  
Tel. +91 22 493 8541, Fax. +91 22 493 0966

**Indonesia:** PT Philips Development Corporation, Semiconductors Division,  
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,  
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,  
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,  
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,  
Tel. +82 2 709 1412, Fax. +82 2 709 1415

**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
Tel. +60 3 750 5214, Fax. +60 3 757 4880

**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

**Middle East:** see Italy

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Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Pakistan:** see Singapore

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106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Ul. Lukiska 10, PL 04-123 WARSZAWA,  
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Tel. +7 095 755 6918, Fax. +7 095 755 6919

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**Slovakia:** see Austria

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2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,  
Tel. +27 11 470 5911, Fax. +27 11 470 5494

**South America:** Al. Vicente Pinzon, 173, 6th floor,  
04547-130 SÃO PAULO, SP, Brazil,  
Tel. +55 11 821 2333, Fax. +55 11 821 2382

**Spain:** Balmes 22, 08007 BARCELONA,  
Tel. +34 93 301 6312, Fax. +34 93 301 4107

**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH,  
Tel. +41 1 488 2741 Fax. +41 1 488 3263

**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,  
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

**Thailand:** PHILIPS ELECTRONICS (THAILAND) Ltd.,  
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,  
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**Turkey:** Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,  
Tel. +90 212 279 2770, Fax. +90 212 282 6707

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
Tel. +1 800 234 7381, Fax. +1 800 943 0087

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**Yugoslavia:** PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,  
Tel. +381 11 62 5344, Fax. +381 11 63 5777

**For all other countries apply to:** Philips Semiconductors,  
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,  
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